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HARRINGTON & SMITH, LLP
4 RESEARCH DRIVE
SHELTON, CT 06484-6212

EXAMINER	
PATEL, HETUL B	
ART UNIT	**PAPER NUMBER**
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,721	ASHMORE ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-32 and 34-37* is/are rejected.

7)☒ Claim(s) *33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the communication filed on December 19, 2005. Claims 1, 7, 12, 17, 19-20, 23-24 and 31 are amended, claim 5 is cancelled, claims 32-37 are newly added and therefore, claims 1-4 and 6-37 are pending in this application.

2. Applicant's arguments with respect to claims 11 and 28 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

3. Claim 1 is objected to because of the following informalities:

It is not clear by the phrase "saving internal state information by the first controller" of claim 1 that whether the first controller is saving the internal state information of the first controller or the other controller(s)?

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1-4, 6-10, 13-15, 20-21, 24 and 29 are rejected under 35 U.S.C. 102(a) as being anticipated by the 'Background of the Invention' section of the current application, hereinafter, BOI.

As per claim 1, BOI teaches a computer program product stored on a computer readable storage medium for maintaining data access during failure of a first controller in a multiple controller storage subsystem, the storage subsystem having an array of data storage devices (i.e. RAID) and at least one other controller for managing the data storage, comprising computer readable program code for performing: the first controller instructing the at least one controller to save the at least one other controller's internal state information (i.e. "the [first] controller detecting a problem can be set up to send a stop message to all other controllers. The other controllers then do a state save [operation]" lines 13-14 on page 2 of BOI); saving internal state information by the first controller (i.e. "to copy the [first] controller's internal state information at the time of the error", lines 8-9 on page 2 of BOI); the first controller resetting itself after the saving of its internal state information (i.e. "[the first controller] copies the [first] controller's internal state information at the time of the error. This data is stored at a predetermined location by the [first] controller before it resets itself" lines 8-10 on page 2 of BOI); pausing operation of the at least one other controller (i.e. "send a stop message to all other controllers" lines 13-14 on page 2 of BOI); the at least one other controller for saving internal state information at the time of pausing, in parallel with the first controller's saving of its internal state information (i.e. a stop message to all other controllers. The other controllers then do a state save [operation]" lines 13-14 on page 2 of BOI); and

continuing operation of the at least one other controller (i.e. "the other controllers will then do a state save before resetting to recover" lines 14-15 on page 2 of BOI) (e.g. see lines 5-19 on page 2 of BOI), wherein only the first controller resets (i.e. "... only the defective [first] controller resets" line 27 on page 2 of BOI), wherein the first and the at least one other controller make the array of data storage devices appear to a host computer as a single high capacity storage device (i.e. "The [first and the at least one other] controllers make the array of data storage devices appear to a host computer as a single high capacity storage device", lines 25-26 on page 1 of BOI).

As per claims 20 and 24, see arguments with respect to the rejection of claim 1. Claims 20 and 24 are also rejected based on the same rationale as the rejection of claim 1.

As per claim 2, BOI teaches the claimed invention as described above and furthermore, BOI teaches that the first controller detects an error (i.e. a problem) in the first controller, which triggers the saving of the internal state information (i.e. by performing a state save step) (e.g. see lines 13-19 on page 2 of BOI).

As per claim 3, BOI teaches the claimed invention as described above and furthermore, BOI teaches that a host computer issues a transaction to the first controller which causes the first controller to save its internal state information (i.e. storing controller internal state information at the time of the error at a predetermined location) (e.g. see lines 5-11 on page 2 of BOI).

As per claim 4, BOI teaches the claimed invention as described above and furthermore, BOI teaches that the first controller resets after saving its internal state

information (i.e. storing controller internal state information at the time of the error at a predetermined location before it resets itself) (e.g. see lines 5-11 on page 2 of BOI).

As per claim 6, BOI teaches the claimed invention as described above and furthermore, BOI teaches that the at least one other controller (i.e. sends message to all other controllers) pauses operation, saves internal state information at the time of pausing, and continues operation (i.e. all other controllers do a state save before resetting to recover) when the at least one other controller detects a loss of the first controller (i.e. when detects a problem in the first controller) such that access to the array of data storage devices is maintained (e.g. see lines 13-19 on page 2 of BOI).

As per claims 7 and 13, BOI teaches the claimed invention as described above and furthermore, BOI teaches that the first controller and the at least one other controller each save their internal state information (i.e. including a subset of the internal state information) to a storage location (i.e. to a predetermined location) corresponding to that controller (e.g. see lines 5-19 on page 2 of BOI).

As per claims 8 and 10, BOI teaches the claimed invention as described above and furthermore, BOI teaches that the first controller and the at least one other controller save their internal state information to the storage devices, i.e. including at least one storage device (i.e. the physical disk(s)) (e.g. see lines 13-19 on page 2 of BOI).

As per claim 9, BOI teaches the claimed invention as described above and furthermore, BOI teaches that the first controller instructs the at least one other

controller to transfer internal state information to the first controller, i.e. other controllers dumps the info to the first controller (e.g. see lines 13-19 on page 2 of BOI).

As per claim 14, BOI teaches the claimed invention as described above and furthermore, BOI teaches that the internal state information saved by the at least one other controller is determined by an instruction received from the first controller (e.g. see lines 13-19 on page 2 of BOI).

As per claim 15, BOI teaches the claimed invention as described above and furthermore, BOI teaches that problem analysis regarding an error in the first controller is carried out on the saved internal state information, i.e. the saved internal state information is used to solve the defect in the first controller (e.g. see lines 5-28 on page 2 of BOI).

As per claim 21, BOI teaches the claimed invention as described above. The further step of retrieving the internal state info stored in the at least one storage device is inherently embedded in the storage subsystem taught by BOI. The internal state information have to be retrieved from the storage device so if one or more of the controllers fail(s), the other controller(s) can use the retrieved state information of the failed controller(s) in order for not to render the system inoperative or any of the data stored in the system inaccessible.

As per claim 29, BOI teaches the claimed invention as described above. The further limitation of having a processor in each of the first controller and the at least one other controller is inherently embedded in the storage subsystem taught by BOI. Every controller has to have a processor/cpu in it to function. The Examiner would like to

introduce Oldfield et al. (USPN: 2002/0133743) as an extrinsic evidence to show that each controller comprises a processor (e.g. see 54 and 60 Fig. 1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 11 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over BOI in view of Fujimoto et al. (USPN: 6,477,619) hereinafter, Fujimoto.

As per claims 11 and 28, BOI teaches the claimed invention as described above, but does not clearly teach that the first controller and the at least one other controller are combined on a single circuit card. Fujimoto, on the other hand, teaches about integrating a plurality of disk array controller in a single disk array controller (e.g. see the abstract and Fig. 5). Accordingly, it would have been obvious to one ordinary skilled in the art at the time of the current invention was made to integrate BOI's first controller and the at least one other controller on a single circuit board as taught by Fujimoto. In doing so, the deterioration of performance due to the data transfer between the disk array control units is alleviated, when the multiple disk array control units are to be operated as a single disk array controller.

6. Claims 16-17, 22, 25 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over BOI in view of Otterness et al. (USPN: 6,601,138) hereinafter, Otterness.

As per claims 16, 25 and 30, BOI teaches the claimed invention as described above but failed to teach that the storage subsystem comprises a Fibre Channel Arbitrated Loop system and the at least one other controller comprises a host bus adapter. Otterness, however, discloses that the storage subsystem comprises a high-speed channel, such as, fibre channel (FC-AL), small computer system interface (SCSI) and memory interconnect, as communication path connected directly between controllers and the at least one other controller comprises a host bus adapter (HBA) (e.g. Col. 7, line 62 –Col. 8, line 2 and claim 1). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement Otterness's FC-AL and HBA in the storage subsystem taught by BOI so the controllers can communicate between each other at high-speed using the high-speed channel.

As per claim 17, the combination of BOI and Otterness teaches the claimed invention as described above and furthermore, BOI teaches that upon detection of a problem in the first controller, it sends a stop message to all other controllers, i.e. it will also disable the interrupts on the other controllers (e.g. see lines 13-19 on page 2 of BOI).

As per claim 22, BOI teaches the claimed invention as described above. However, BOI failed to teach that the first controller and the at least one other controller

share a single memory. Otterness, on the other hand, teaches about using a shared-memory controller so the tokens can be dynamically distributed to be executed by the memory controllers (e.g. see Col. 3, lines 5-11). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement Otterness' shared-memory controller, i.e. sharing a single memory between memory controllers, in the storage subsystem taught by BOI so a failure of one or more of the controllers does not render the system inoperative or any of the data stored in the system inaccessible.

7. Claims 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over BOI in view of Otterness, further in view of Skazinski et al. (USPN: 6,574,709) hereinafter, Skazinski.

As per claim 18, the combination of BOI and Otterness teaches the claimed invention as described above. However, none of them clearly teach about setting a flag to prevent overlapping saves of internal state information in that adapter. Skazinski teaches that using alternate flag (see line 8, Table 6) which is set to equal to true ("1"), to indicate that an alternate mirror entry 6000 is being used to perform the present mirror cache operation to prevent the problems with respect to mirror operation overlap (e.g. see Col. 22, lines 40-47). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement Skazinski's step of setting the flag in the system taught by BOI and Otterness to avoid overlapping saves of internal state information in that adapter.

8. Claims 19 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over BOI in view of Otterness, further in view of Vishlitzky et al. (USPN: 6,047,353) hereinafter, Vishlitzky.

As per claim 19, the combination of BOI and Otterness teaches the claimed invention as described above. However, none of them clearly teach that the host bus adapter saves information relating to an interface chip. Vishlitzky, on the other hand, teaches that the host bus adaptor (i.e. 24 in Fig. 2) save information relating to an interface chip trace area (in the trace buffer 30 in Fig. 2) (e.g. see Fig. 2). Accordingly, it would have been obvious to one ordinary skilled in the art at the time of the current invention was made to implement the trace buffer to store the trace information as taught by Vishlitzky in the computer program product taught by the combination of BOI and Otterness. In doing so, (i) host activity can be synchronized with the disk activity; and (ii) using the trace info from the trace buffer, the failure of the controller can be debugged.

As per claim 23, see arguments with respect to the rejection of claims 1, 17 and 19. Claim 23 is also rejected based on the same rationale as the rejection of claims 1, 17 and 19.

9. Claims 12, 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over BOI in view of Oldfield et al. (USPN: 2002/0133743) hereinafter, Oldfield.

As per claim 12, BOI teaches the claimed invention as described above but failed to teach the further limitation of saving external memory data, in addition to the internal

state information by at least one of the first controller and the at least one other controller. Oldfield, on the other hand, discloses about saving the external memory data, i.e. the mirrored memory data in at least one of the first controller and the at least one other controller (e.g. see paragraph [0035] on page 3). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement Oldfield's teachings in the storage subsystem taught by BOI. In doing so, if the first controller fails, then the at least one other controller can take over the responsibilities of the first controller without affecting the functionality of the subsystem. Therefore, it is being advantageous.

As per claim 26, BOI teaches the claimed invention as described above but failed to teach that at least one of the first controller and the at least one other controller comprises a memory buffer. Oldfield, however, teaches that each controller comprises a memory buffer (i.e. 138 and 178 in Fig. 4). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the memory buffer as taught by Oldfield in the storage subsystem taught by BOI so predefined background tasks can be processed without interrupting the processing of system operation commands via system operation processor (e.g. see paragraph [0043]).

As per claim 27, BOI teaches the claimed invention as described above but failed to teach the further limitation of sharing an external memory by the controller and the at least one other controller. Oldfield, on the other hand, teaches that the controller and the at least one other controller shares an external memory (e.g. see paragraph [0051]).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement Oldfield's teachings in the storage subsystem taught by BOI so the memory self-test can be performed upon the insertion of the controller.

10. Claim 31 and 34-37 is rejected under 35 U.S.C. 103(a) as being unpatentable over DeKoning et al. (USPN: 5,933,824) hereinafter, DeKoning in view of BOI, further in view of Okazaki (USPN: 6,345,332).

As per claim 31, DeKoning teaches a Fibre Channel Arbitrated Loop (FC-AL) storage system (shown in Fig. 2) comprising a first set of disk drives (208.1 in Fig. 2) connected to a first set of loops (150.1 in Fig. 2), and a second set of disk drives (208.2 in Fig. 2) redundant with the first set of disk drives and connected to a second set of loops (150.2 in Fig. 2); wherein a first adapter (202.1 in Fig. 2) is connected to the first set of loops and a second adapter (202.2 in Fig. 2) is connected to the second set of loops. However, DeKoning failed to teach that each adapter being adapted for issuing a command to the other adapter to save internal status data and each adapter adapted for saving internal status data and resetting. BOI, on the other hand, teaches that in case if a controller (adapter) detects a problem, it sends a stop message to all other controllers (adapters); all other controllers saves their internal states and resets before recovering (e.g. see lines 13-19 on page 2 of BOI). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the teachings of BOI in the FC-AL storage system taught by DeKoning so the

recovery action can be performed on the failed adapter without loosing the data of the other adapters.

However, both DeKoning and BOI failed to teach that each adapter being adapted for issuing a command to the other adapter to save internal status data and not reset itself. Okazaki, on the other hand, teaches about locating the faulty location and resetting only that faulty location without resetting the dual system as a whole (e.g. see Col. 13, lines 60-65). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the teaching of Okazaki in the system taught by the combination of DeKoning and BOI. In doing so, faults are corrected (i.e. on a faulty adapter) without interrupting services provided by the dual system (i.e. by the other adapter(s)). Therefore, it is being advantageous.

As per claims 34-37, the combination of DeKoning, BOI and Okazaki teaches the claimed invention as described above. The system dump feature is well-known and notorious old in the art at the time of current invention was made. The two types of system dumps comprises the dump to disk, which stores all internal status data at the time of an unusual system error and resets the system; and the live dump stores all internal status data at the time of an unusual system error without resetting. It is also well-known and notorious old at the time of current invention was made that FC-AL storage system has a fibre context and an interrupt context. It is well-known that by using the live dump feature, when a storage adaptor fails in RAID system and one of the first and second adapters live dumps, it sends a message to an other of the first and

second adapters to build a data structure recording state information for debugging purposes. The Examiner herein taking Official Notice on this subject matter.

11. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over DeKoning et al. (USPN: 5,933,824) hereinafter, DeKoning in view of BOI, further in view of Okazaki, further in view of Kahle et al. (USPN: 5,758,120) hereinafter, Kahle.

As per claim 32, the combination of DeKoning, BOI and Okazaki teaches the claimed invention as described above. However none of them teaches the further limitation of setting a flag when internal status data save operation is occurring to prevent another internal status data save operation from being invoked. Kahle teaches that a flag (i.e. the indicator bit) is set when internal status data save operation is occurring to prevent another internal status data save operation from being invoked, i.e. prohibiting simultaneous accesses (e.g. see Col. 8, lines 16-24). Accordingly, it would have been obvious to one ordinary skilled in the art at the time of the current invention was made to implement the teaching of Kahle in the storage system taught by the combination of DeKoning, BOI and Okazaki so the data corruption and/or data loss is avoided by prohibiting simultaneous accesses by setting the indicator bit.

Allowable Subject Matter

12. Claim 33 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Remarks

13. As to the remark, Applicant asserted:

(a) The BOI neither discloses nor suggests that a first controller's internal state information is saved and at least one other controller's internal state information is saved without resetting the at least one other controller.

(b) Neither the BOI not Okazaki, alone or in combination, disclose or fairly suggest the first and other storage controllers storing their internal state information where only the first storage controller resets.

(c) Applicant challenges the taking of Official Notice and requests an appropriate teaching (i.e. a reference) and motivation (e.g. preferably from that reference) be provided for these limitations.

(d) BOI does not appear to disclose or even suggest "interrupts are disabled" as recited in claim 17.

(e) None of BOI and Otterness clearly teach about setting a flag to prevent overlapping saves of internal state information in that adapter.

(f) Skazinski does not disclose setting a flag to prevent overlapping saves of internal state data in that adapter. Skazinski also appears to be concerned with host write data (e.g. column 14, lines 35-48) and not state information, as claimed.

(g) Neither Otterness nor the BOI seem to disclose the use of flags.

(h) Mason does not disclose or suggest that the host bus adapter saves information relating to an interface chip trace area.

(i) Neither the BOI nor Okazaki, alone or in combination, disclose or fairly suggest the first and other storage controllers storing their internal state information where only the first storage controller resets.

Examiner respectfully traverses Applicant's remark for the following reasons:

With respect to (a)-(b) and (i), since the BOI teaches that the other controllers first pausing the operation by getting a stop message, second do a state save and third resetting to recover, the resetting step does not occur at the time of the pausing step, i.e. the other controllers save internal state information without resetting at the time of pausing as claimed. BOI also teaches that in other embodiment, only the first controller resets (i.e. "... only the defective [first] controller resets" line 27 on page 2 of BOI).

With respect to (c), Fujimoto prior art is presented in response to the Applicant's challenge regarding the Official Notice that was taken in previous Office Action for a well-known feature. Fujimoto prior art teaches about integrating a plurality of disk array controller in a single disk array controller (e.g. see the abstract and Fig. 5). It would have been obvious to one ordinary skilled in the art at the time of the current invention was made to integrate BOI's first controller and the at least one other controller on a single circuit board as taught by Fujimoto. In doing so, the deterioration of performance due to the data transfer between the disk array control units is alleviated, when the multiple disk array control units are to be operated as a single disk array controller.

With respect to (d), BOI teaches that upon detection of a problem in the first controller, it sends a stop message to all other controllers (e.g. see lines 13-19 on page

2 of BOI). If the other controllers are stopped/paused from operation as a result of the stop message, the interrupts on the other controllers automatically get disabled.

With respect to (e)-(g), Skazinski does clearly teach about using alternate flag (see line 8, Table 6) which is set to equal to true ("1"), to indicate that an alternate mirror entry 6000 is being used to perform the present mirror cache operation to prevent the problems with respect to mirror operation overlap (e.g. see Col. 22, lines 40-47). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement Skazinski's step of setting the flag in the system taught by BOI and Otterness to avoid overlapping saves of internal state information in that adapter.

With respect to (h), Examiner agreed with Applicant that Mason does not disclose the host bus adapter saves information relating to an interface chip trace area. Vishlitzky, however, teaches that the host bus adaptor (i.e. 24 in Fig. 2) save information relating to an interface chip trace area (in the trace buffer 30 in Fig. 2) (e.g. see Fig. 2).

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Ashida et al. (USPN : 6,598,108) teaches about integrating a plurality of controllers on a integrated controller.

- Chong Jr. et al. (USPN : 6,651,131) also teaches about integrating a plurality of storage controllers on a single I/O card (e.g. see claim 2).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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HONG CHONG KIM
PRIMARY EXAMINER